Ultra-low dc Power GaAs HBT S-band Low Noise Amplifiers

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ABSTRACT

We report on a 2.1 mW low dc power GaAs HBT LNA with 2.0 dB noise figure and 8.9 dB gain at 2 GHz. This amplifier achieves a Gain/NF•P_{dc} ratio figure of merit of 2.10 (1/mW) which is the highest reported at S-band. Under low dc power bias of 2V and 0.46 mA (0.92 mW), the amplifier achieves 5.2 dB gain, 3.01 dB noise figure and a Gain/P_{dc} figure of merit of 5.65 (dB/mW) which is also the highest reported in this frequency band. The HBT LNA consumes an area of 1.05x0.82 mm^2 and is fabricated using a relaxed 3 μm emitter width low cost GaAs production foundry process. The high performance obtained from HBTs at very low dc bias makes them attractive for portable wireless consumer applications.

I. Introduction

GaAs HBTs are attractive for portable consumer applications because of their high device transconductance under low dc bias, small size, and low device noise figures at L- and S-band frequencies. A previously reported ultra-low dc power GaAs HBT amplifier achieved 13.1 dB gain with 5 mW of dc power, and a record gain to dc power ratio (Gain/P_{dc}) of 2.6 dB/mW at X-band[1]. However, no previous results on the noise and gain performance of an ultra-low dc power HBT L- or S-band amplifier has been reported until this work. Fig. 1 shows a graph of Gain:P_{dc} ratio plotted versus noise figure for several state-of-the-art L- and S-band LNAs [2-9]. A Gain/P_{dc} ratio of 19.1 was demonstrated with MESFET technology and is the highest reported to date. However, this is at a frequency of 1.25 GHz (L-band) and the corresponding noise figure is 6 dB[2]. The HBT LNA of this work obtained Gain/P_{dc} ratios of 4.2 and 5.65 at 2.0 GHz which are the highest reported at S-band, and achieves noise figures of 2.0 dB and 3.01 dB, respectively.

For portable consumer applications there is a performance-size(cost) trade-off which can be illustrated by plotting chip size versus Gain/NF•P_{dc} ratio which is a figure of merit measuring the utility of an LNA for low power applications[6]. Fig. 2 shows a plot

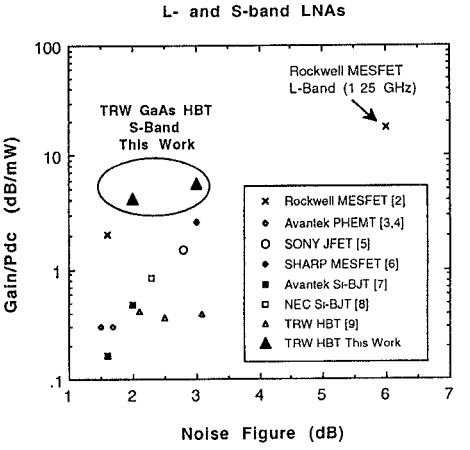

Fig. 1 Gain to dc power ratio plotted versus noise figure for several state-of-the-art L- and S-band LNAs.

of chip size versus Gain/NF•P_{dc} ratio for the various L- and S-band LNAs. This figure illustrates that higher performance is achieved at the expense of larger chip size. Fig. 2 also shows that a MESFET LNA achieves a Gain/NF•P_{dc} ratio of 3.0 (1/mW) which is the highest reported at L-band. The GaAs HBT LNA of this work achieves a Gain/NF•P_{dc} ratio of 2.1 (1/mW) which is the highest

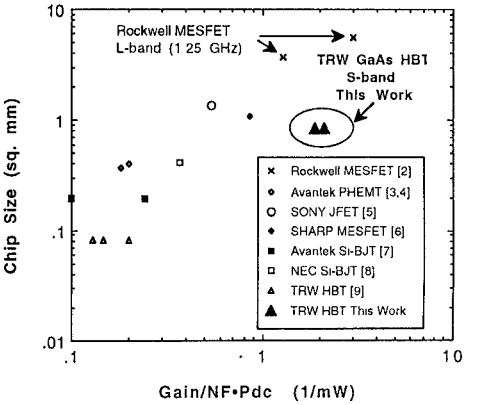

Fig. 2 Chip size versus Gain/NF•P_{dc} ratio for the various L- and S-band LNAs.

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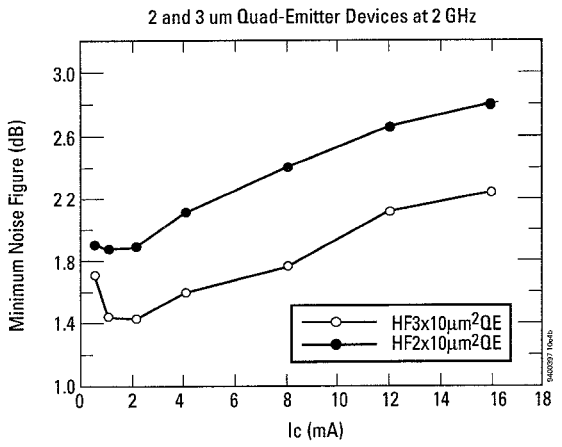

Fig. 3 Minimum noise figure of both 2- and 3-μm HBT quad-emitter devices as a function of collector current at 2 GHz.

reported at S-band, and is 4-5 times smaller in area than the L-band MESFET LNA. The HBT LNA is < 1mm^2 and is comparable in size to several of the other L-band LNA chips which have much poorer Gain/NF•P_{dc} ratio figure of merits Thus, the HBT LNA of this work compacts high performance in a much smaller area.

II. GaAs HBT Low Noise Process Technology

The LNA was fabricated with TRW's AlGaAs/GaAs HBT foundry technology. The MBE profile of our standard GaAs HBT process incorporates a base thickness of 1400Å uniformly doped to 1x10^{19} cm^{-3}, a collector thickness of 7000Å lightly doped N-type of 7x10^{15} cm^{-3}, and an N$^+$ sub-collector doped to 5x10^{18} cm^{-3}. The HBT process incorporates a Self-aligned Base Ohmic Metal (SABM) technique for fabricating both 2- and 3-μm emitter width HBTs. The resulting HBT transistors have an f_T and f_{max} of 23 GHz and 50 GHz, respectively.

Noise parameters were measured for a 2x10 μm^2 and a 3x10 μm^2 HBT quad-emitter device. Fig. 3 gives the minimum noise figure of both the 2- and 3-μm HBT devices as a function of collector current at 2 GHz. Over bias current, a 0.5 dB improvement in device minimum noise figure is seen for the 3-μm HBT over the 2-μm HBT device. The noise improvement using the 3-μm HBTs may be explained by the lower emitter contact resistance which results in lower thermal noise. The drawback of the 3-μm HBTs is that they will have poorer amplifier frequency capability due to the larger junction capacitances and higher base resistance. Fig 3 also illustrates that as the collector bias current is decreased, the minimum noise figure of both HBT devices decreases until a collector current of about 2 mA is reached. From 2 mA down to 0.5 mA the minimum noise figure of the devices levels off. This bias dependent characteristic was also observed at 1 and 3 GHz. For HBT devices, lower current generally means lower minimum noise, however, for low noise amplifier design, the source impedance required to achieve minimum noise (gamma opt) needs to be considered over bias. This point is especially important for amplifiers which extend into the microwave frequency range.

Fig. 4 shows a plot of the optimum noise source impedance (gamma opt.) from 300 MHz to 3 GHz of a 3x10 μm^2 quad-emitter HBT as a function of collector current. The impedance plot shows that at lower currents the optimum impedance has a large real part, greater than 50 ohms, with a significant inductive reactance.

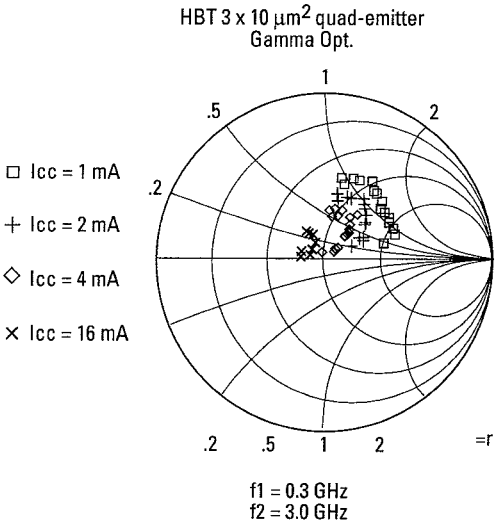

Fig. 4 Optimum noise source impedance (gamma opt.) loci plotted from 300 MHz to 3 GHz of a 3x10 μm^2 quad-emitter HBT device for several different collector currents.

For higher collector currents, gamma opt. is mostly real and decreases below 50 ohms. At 16 mA, the impedance is close to 50 ohms over the frequency range. At this bias point, the gamma opt. is nearly coincident with 50 ohms which makes it easier to design both good input return-loss and low noise figure over a broad band, however the minimum achievable noise figure at this bias will be higher than at lower bias currents. For low noise and low dc bias operation, a design employing series inductive matching at the input of the HBT device will result in optimum noise match over a narrow band. The design of a 2.0 GHz L-band amplifier is described below.

III. S-band HBT Low Noise Amplifier

A schematic of the 2 GHz low dc power, low noise HBT amplifier is shown in Fig. 5. The amplifier is a one-stage narrow-band design which is matched for a center frequency of 1.9-2.0 GHz. An input series inductor, L_b, is used to match the input of a 3x10 μm^2 quad-emitter for minimum noise A collector bias current of 1 mA and a V_{ce}=2.0 V was chosen in order to realize a gain greater than 8 dB and a minimum noise figure less than 2.0 dB

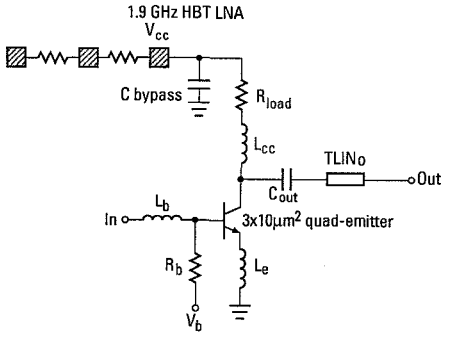

Fig. 5 Schematic of the 2 GHz low dc power, low noise HBT amplifier.

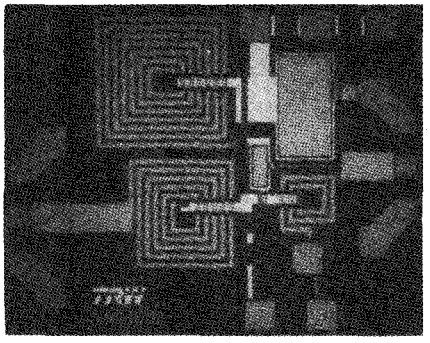

Fig. 6 Microphotograph of the 1.9 GHz single stage low noise amplifier chip. The total chip area is 1.05x0.82 mm^2.

with a total power consumption of 2 mW at 2 GHz. An inductor L_e, in series with the emitter of the HBT device is used to tune gamma opt so that it coincides more closely to the 50 Ω source impedance in order to achieve optimum noise and input return-loss match. This is a conventional low noise microwave matching technique which is common among MESFET and HEMT LNA designs. The output of the amplifier is matched using a series L-C matching network comprised of C_{out} and $TLIN_O$. An inductive choke L_C, in series with a small load resistance, R_{load}, provides both a high pass ac load and a means for biasing the collector of the HBT device.

Fig. 6 shows a microphotograph of the 2.0 GHz single stage low noise amplifier chip which is 1.05x0.82 mm^2 in area. Square inductors were used to minimize the required area of the passive components. Much of the wasted area is consumed by 50 Ω transmission lines and on-wafer rf probe pad configurations. A production layout of this chip can be reduced by 40 %, including the self-biasing network.

IV. Measured Results

Noise figure and gain were measured at different bias conditions in order to find the optimum noise bias of the amplifier. Fig. 7 shows gain and noise figure performance at 2 GHz as a function of voltage (V_{cc}) for a fixed collector current, I_{cc}= 5 mA.

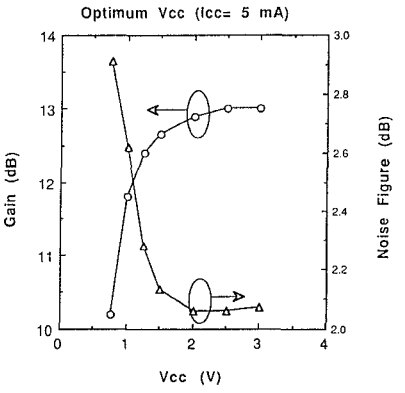

Fig. 7 Gain and noise figure performance at 2 GHz as a function of bias voltage V_{CC} (I_{CC} = 5 mA).

This figure shows that at a $V_{CC} \geq 2.0$ V, the amplifier achieves minimum noise figure and maximum gain performance. This may be explained by the fact that the collector-base capacitance is fully depleted under reverse biases of greater than about 0.6 Volts which corresponds to a $V_{CC} \approx V_{ce}$= 2.0V. This characteristic is dependent on the material structure of the collector and base of the HBT. At this optimum collector voltage, the gain and noise figure were measured as a function of collector bias current (I_{CC}) at 2 GHz, and is given in Fig. 8. This figure shows that the optimum low noise bias current (I_{CC}) is between 2 mA and 4 mA for the HBT LNA. At currents slightly lower than 2 mA the noise figure begins to ramp up very quickly due to a rapid change in the gamma opt over bias. A figure of merit which measures the utility of an LNA under low dc power consumption is the Gain/NF•P_{dc} ratio (1/mW) and has been previously defined[6]. At an optimum collector bias of 1.04 mA and 2.1 mW power consumption, the corresponding Gain/NF•P_{dc} ratio figure of merit is 2.10 (1/mW) which is the highest reported at S-band for any technology.

Fig. 9 shows the measured gain, noise figure, and return-loss of the amplifier at optimum low noise bias (I_{CC}= 2 mA and a V_{CC}= 2.0V). The nominal gain is 11.1 dB at 2.0 GHz with a corresponding input and output return-loss of -13.7 dB and -14.7 dB, respectively. The amplifier has a 40 % 1-dB bandwidth from 1.5-2.3 GHz. Fig. 9 also shows the broadband noise figure performance. Over a 1.5-2.8 GHz bandwidth, the noise figure ranges from a minimum of 1.9 dB to a maximum of 2.2 dB. Under a very low dc collector current bias of 0.46 mA and a total power consumption of 0.92 mW through 2 Volts, the gain and noise figure are 5.2 dB and 3.1 dB, respectively, at 2 GHz. At this low dc bias, the gain:P_{dc} ratio is 5.65 dB/mW which is also the highest reported for an S-band amplifier.

Fig. 10 gives the $P_{1\text{-}dB}$ output compression and IP3 performance at 2 GHz as a function of collector bias current (I_{CC}). At a low noise bias of 2 mA and V_{CC} = 2.0 Volts, the corresponding

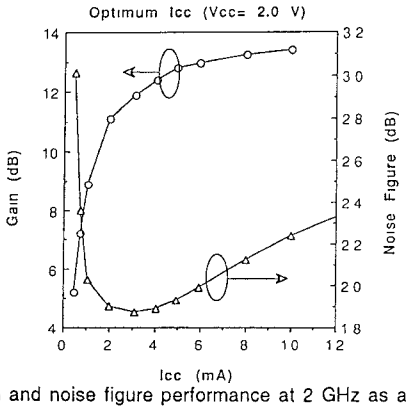

Fig. 8 Gain and noise figure performance at 2 GHz as a function of collector bias current I_{CC} (V_{CC} = 2.0 V).

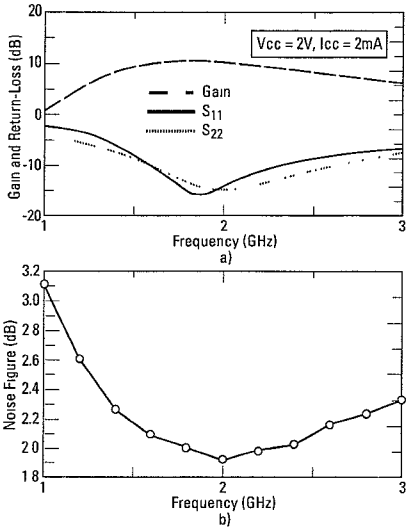

Fig. 9 Measured a) gain and return-loss, and b) noise figure performance at an I_{CC}= 2 mA and a V_{CC}= 2.0 V.

IP3 and $P_{1\text{-}dB}$ are 11 dBm and 0 dBm, respectively. At an ultra-low dc bias of 0.46 mA and Vcc= 2.0 Volts, the corresponding IP3 is -2.8 dBm. The $P_{1\text{-}dB}$ compression was measured for both a V_{CC}= 2.0 and 3.0 Volts as a function of bias current (I_{CC}). At a V_{CC} = 3 Volts, the 1-dB compression was found to be 3-4 dB higher at the higher current bias. Fig. 10 also illustrates that for a fixed V_{CC}=2.0V, the delta between the IP3 and P1-dB is 15 dB. This is greater than the "10 dB delta rule of thumb" assumed for conventional FET amplifiers. This suggests that higher amplifier linearity can be achieved from HBTs at low dc bias.

Conclusion

A 2.1 mW ultra-low dc power GaAs HBT LNA with 2.0 dB noise figure and 8.9 dB gain was achieved at 2 GHz. The corresponding Gain/NF•P_{dc} ratio figure of merit is 2.10 (1/mW) which is the highest reported at S-band. Under low dc power bias of 2V and 0.46 mA, or 0.92 mW of power consumption, the amplifier achieves 5.2 dB gain, 3.01 dB noise figure and a Gain/P_{dc} figure of merit of 5.65 (dB/mW) which benchmarks the highest reported gain to dc power ratio (Gain/P_{dc}) in this frequency band. The high performance obtained from HBTs at very low dc bias, and the low cost nature of GaAs HBT fabrication technology, make HBTs attractive for portable wireless consumer applications.

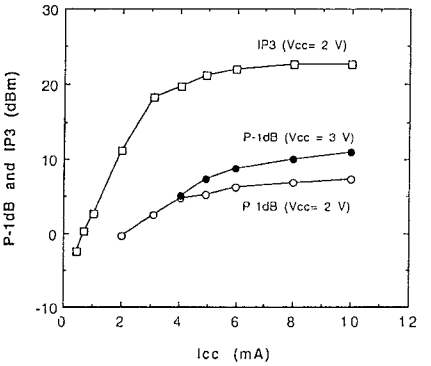

Fig. 10 P_{1dB} output compression and IP3 performance at 2 GHz versus collector bias current, I_{CC}.

Acknowledgement

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